ABSTRACT OF THE DISCLOSURE

A method and apparatus for synchronizing and communicating between processing entities, such as cores or threads, in a multiprocessor. Two registers are used as a "hardware mailbox" by two processing entities of a microprocessor. A first register is used to communicate information from a first processing entity to a second processing entity, while a second register is used to communication information from the second processing entity to the first processing entity. The first and second registers are cross-decoded by the two processing entities. One or more bits in each register are used to synchronize operation of the processing entities. In a microprocessor including three or more such processing entities, a read-write register of each processing entity holds outgoing information and a read-only register of each processing entity holds incoming information. A separate logic circuit logically combines the contents of the read-write registers and stores the result in the read-only registers.